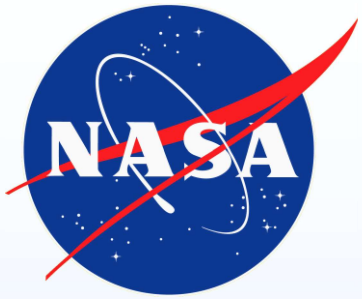

Advanced Micro Devices (AMD) Processor: Radiation Test Results

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Outline

- Background and Motivation
- Device Under Test
- Hardness Assurance Method(s)
- Total Dose Results
- Dose Rate Results
- Analysis
- Summary

Abstract: **Total dose and dose rate evaluations were performed on an Advanced Micro Devices (AMD) state-of-the-art processor (fabrication: 32nm CMOS SOI technology from Dresden, Germany). International Traffic in Arms (ITAR) levels were used as a metric with the device tolerance exceeding these levels.**

CMOS = complementary metal oxide semiconductor; SOI = silicon on insulator

Background and Motivation

- There has been much discussion throughout the government and industry regarding the International Traffic in Arms (ITAR) regulations as they pertain to radiation-induced device tolerance. This is a dual-edged sword:
  - How to protect critical U.S. technologies from unfriendly hands, while at the same time,
  - Commercial semiconductor manufacturers fearing inadvertent exceeding of the ITAR radiation levels.
- By utilizing a representative non-U.S. foundry, the authors sought to evaluate how this semiconductor process would fare against a subset of the ITAR criteria: total dose and dose rate (DR) limits.
- How the testing was performed is of note and discussion for the radiation effects community:
  - The utilization of commercial processor motherboards as tester/bias board and a suite of "stress" tests (software tests that stress the device and measure performance).

Current ITAR Microelectronics Radiation Levels –

Excerpt from THE UNITED STATES MUNITIONS LIST -§ 121.1

- **(d) Radiation-hardened microelectronic circuits that meet or exceed all five of the following characteristics:**
  - **(1) A total dose of 5×10^5 rad(Si);**
  - **(2) A dose rate upset threshold of 5×10^8 rads(Si)/sec;**
  - **(3) A neutron dose of 1×10^{14} n/cm^2 (1 MeV equivalent);**
  - **(4) A single event upset rate of 1×10^{-10} errors/bit-day or less, for the CREME96 geosynchronous orbit, Solar Minimum Environment;**
  - **(5) Single-event latchup (SEL) free and having a dose rate latch-up threshold of 5×10^8 rad(Si).**
- **This effort looked at (1), (2), and part of (5)**

The Device Under Test (DUT)

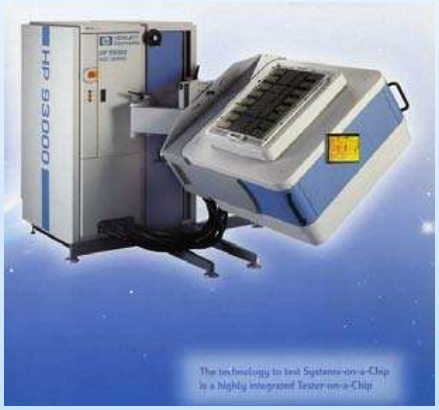
- **The DUT is a modern state-of the-art dual-core processor from Advanced Micro Devices (AMD)**
  - **Part number : AMD A4-Series AD3300OJHXBOX**
  - **Production date code: DA 1153PGN**
  - **This is a 2.5 GHz dual-core processor**
    - **Integrated floating point unit**
    - **Both level 1 and level 2 caches**
    - **Die size: 228 mm^2**
    - **Nominally a 65 Watt thermal design power**
    - **Package: 905-pin lidded micro-Pin Grid Array (µPGA) package**
  - **The device utilizes the Llano processor core with on-chip peripherals including a dual-channel DDR3 memory controller, a PCI Express 2.0 controller and high definition graphics controller**
- **AMD is a fabless semiconductor manufacturer**
  - **This specific device is built on Globalfoundries' 32 nm fab process located in Dresden, Germany**
  - **The process includes hi-K metal gates (HKMGs) on a partially-depleted silicon-on-insulator (PD-SOI) substrate**

AMD A4-3300 series microprocessor

Radiation Test Method – Total Dose

- **Traditional Method**

Custom Bias Board
–
w/ IC sockets and connections to outside the chamber



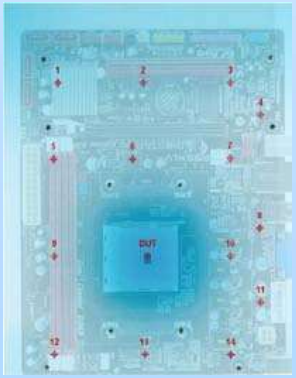
Automated Test Equipment (ATE) w/test vectors

Step irradiations using Bias Board followed by measurements w/ external ATE at TBD intervals

- **Method Utilized Here**

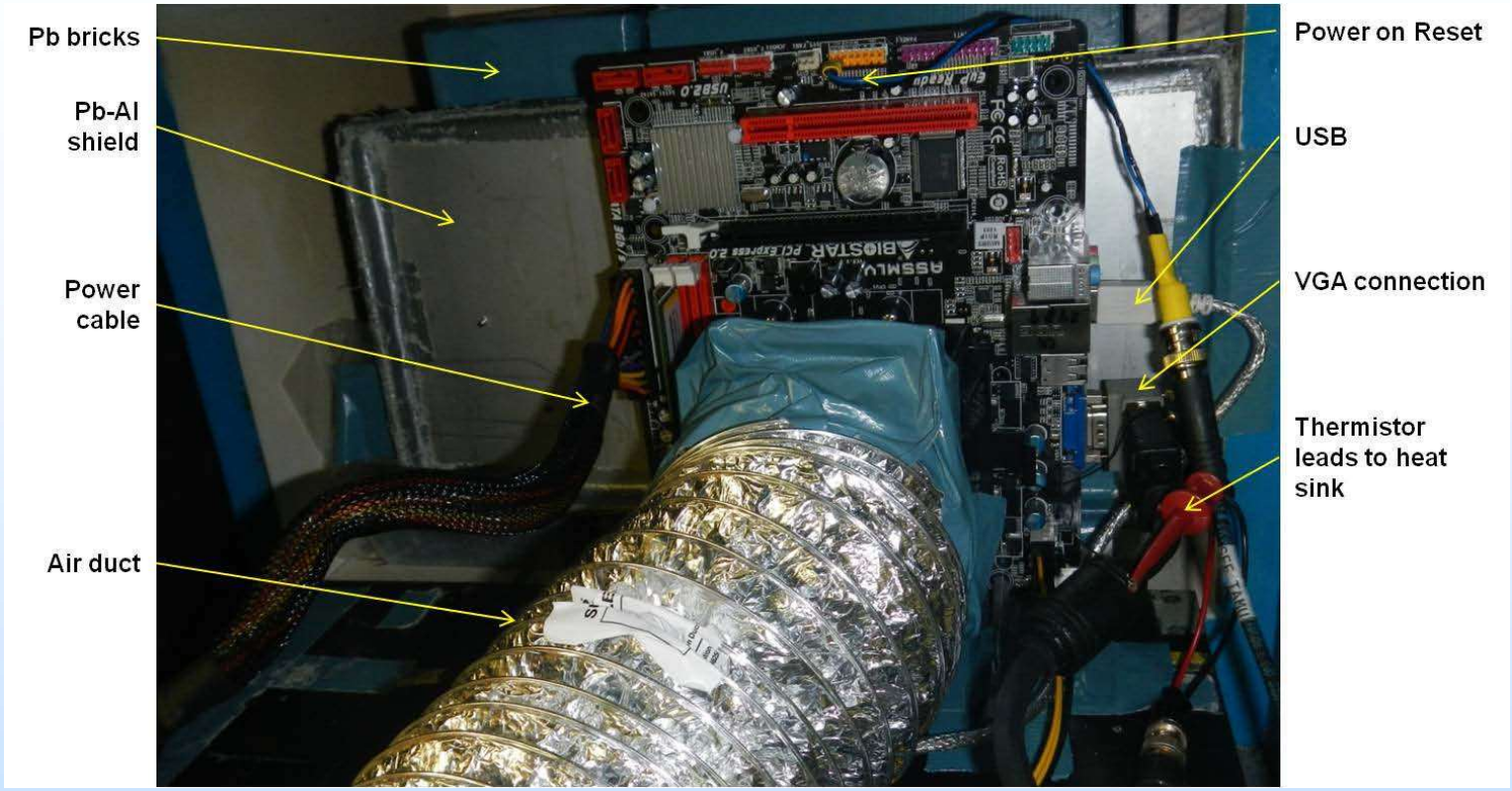
Commercial Biostar A55MLV Motherboard
- one copy used as bias board
- one copy used as "tester" running commercial "freeware" stress tester software

Caveat:
Additional shielding surrounding the processor to minimize exposure levels to non-processor ICs



Sample radiographic film overlay on bias motherboard

Total Dose Test Setup

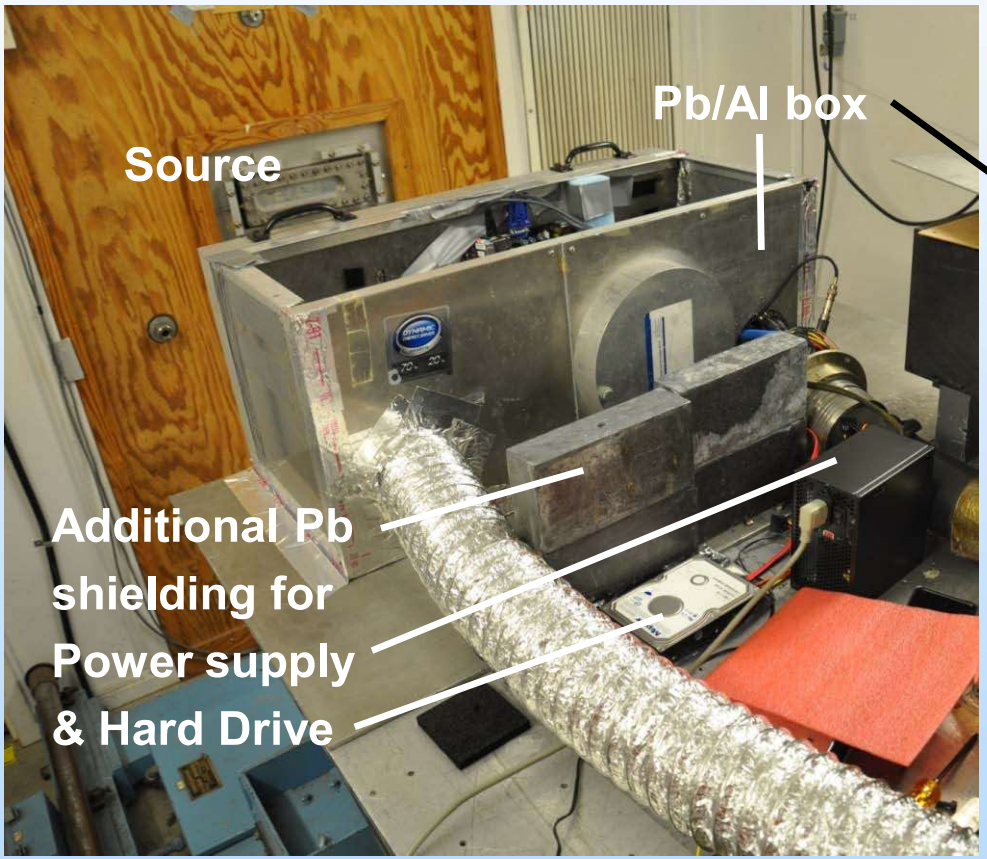


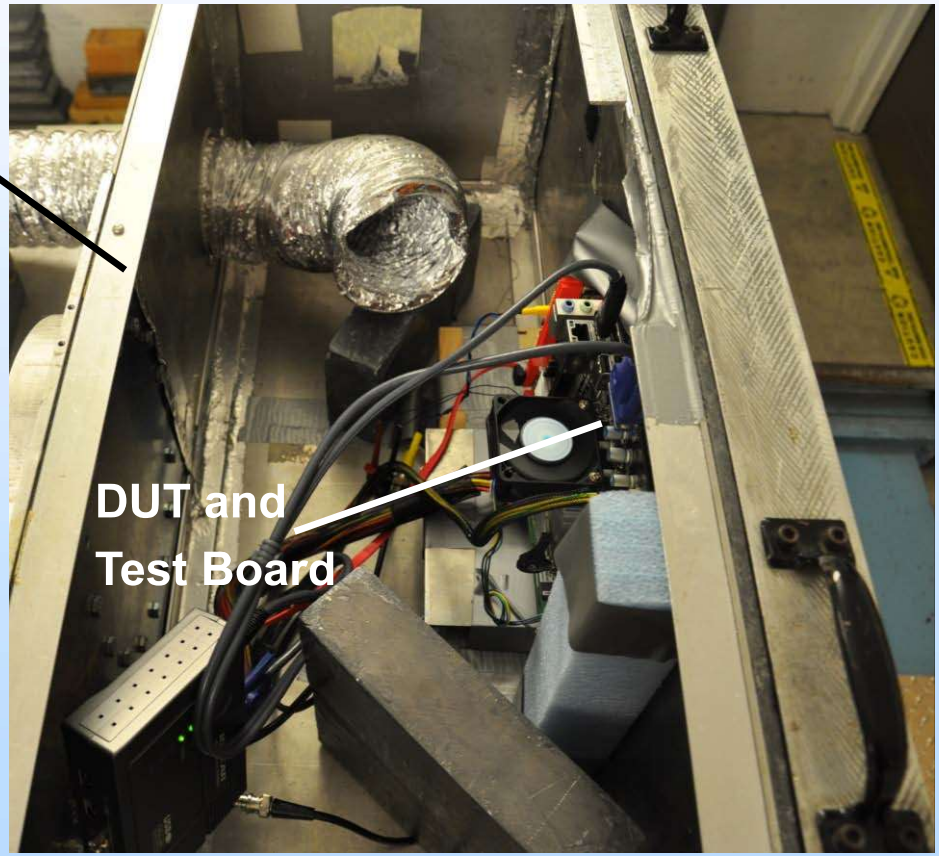
- **Stress software**
  - **1. HWiNFO64. This tool collects and displays information about the hardware configuration. Part of that software function is the ability to monitor and log electrical / environmental data from the motherboard, CPU, GPU and other sensors. This data is recorded for all tests.**
  - **2. IntelBurnTest. This software provides a useful stress testing tool and benchmark. The program is a graphical interface unit (GUI) front-end for a compiled executable that performs math using the Linpack programming library. This tool burdens the CPU workload and enables the user to determine when/if there are flaws in the CPU's ability to perform operations. Inconsistencies due to radiation are recorded.**

CPU = central processing unit; GPU = graphics processing unit

Dose Rate Test Method

- Performed at Crane NAVSEA on 15 August 2012 using the LINAC in electron beam mode
- Exposures made while executing IntelBurn Test S/W

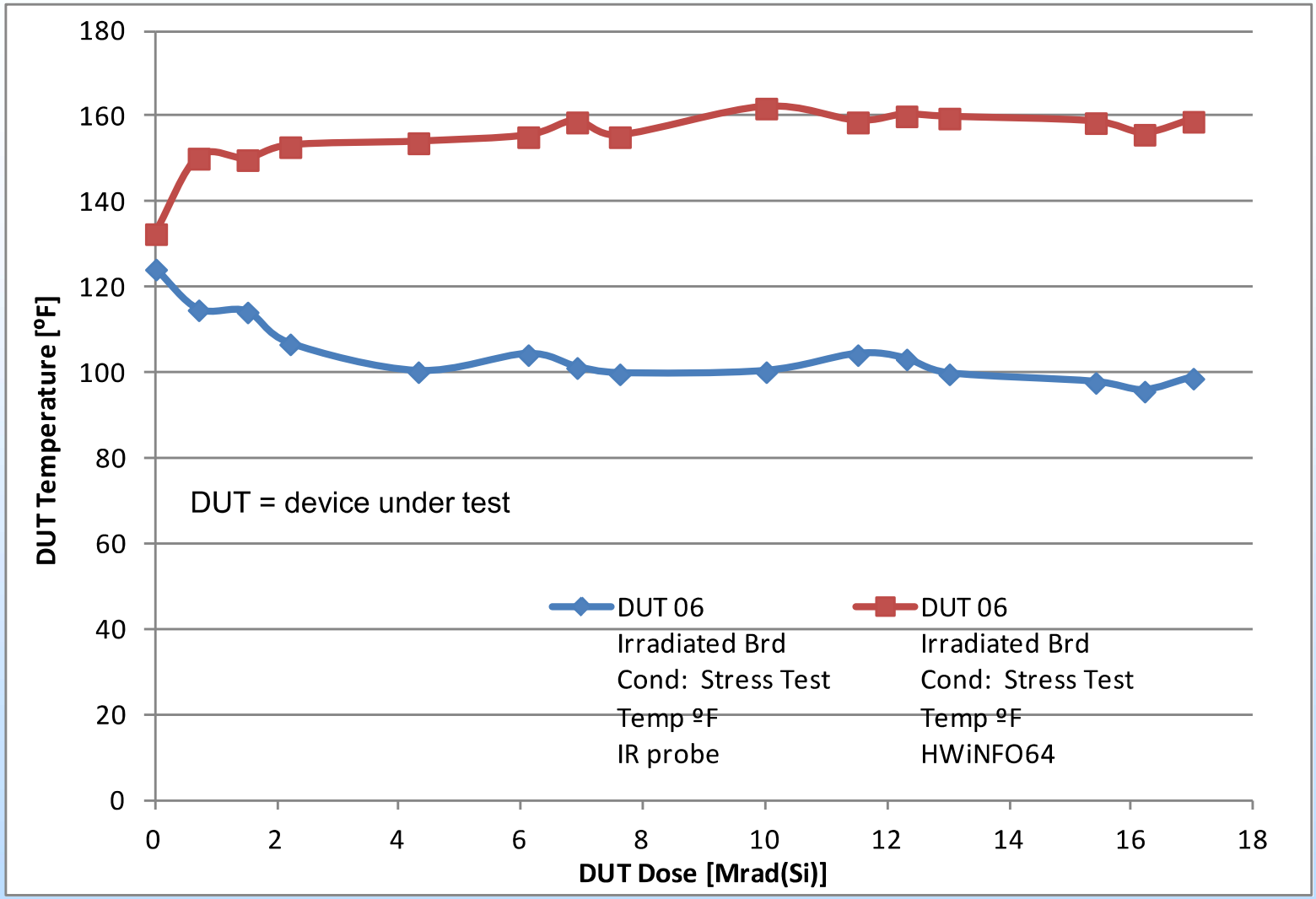




Total Dose Results

- **Bottom line up front:**
  - **3 samples irradiated**
  - **NO processor failures observed (1,4 and 17 Mrad(Si), respectively). "17" is NOT a typo.**
- **However,**
  - **Bias motherboard (though heavily shielded except processor) experienced failures/anomalies**
    - **Surprisingly, DDR3 memory modules failed (though they passed "performance" in a commercial TRIAD memory tester post-irradiation).**
      - **Varied by memory module with 1.1 krad(Si) being lowest failure level.**
    - **Fans degraded at ~ 4 krad(Si) – required motherboard swap**
    - **1 motherboard failed @ 9.7 krad(Si) – entered a "biased, but unknown" state – required motherboard swap**
  - **Temperature "readings" degraded (see next chart)**

Temperature "degradation"



Red line indicates data points using processor's temperature measurement circuit (diode?)

Blue line data using external infrared (IR) thermometer gun

Increased temperature reading likely due to thermal diode or similar degradation

Dose Rate Test Results

- Exposures between $5.6x10^7$ to $2.6x10^{10}$ rad(Si)/sec
- Processor upsets occurred above $1.8 x10^9$ rad(Si)/sec
  - Processor passed all post-exposure software stress tests
- Graphic processor unit (GPU) experienced multiple modes of upset at all tested dose rates
- No dose rate latchup noted up to $2.6x10^{10}$ rad(Si)/sec

rad(Si)/sec	Response To Radiation
$5.6x10^7$	"Blink" - video temporarily blanked out, but independently recovered to normal in 2-3 sec. CPU and GPU stress test continued running. No visible artifacts in GPU window
$1.0x10^8$	"Blink"
$2.4x10^8$	"Blink"
$5.1x10^8$	"Blink"
$1.6x10^9$	"Blink"
$1.8x10^9$	"Blink"
$2.3 x10^9$	CPU turned off; power on reset (POR) to recover
$4.4x10^9$	CPU reset; auto recover
$8.2x10^9$	CPU turned off; POR to recover
$2.6x10^{10}$	CPU turned off; POR to recover

Total Dose Processor "History"

- INTEL 80386-20 (test date: 1993) – 1um CHMOS IV
  - Failure between 5-7.5 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/PPM-93-062.pdf*
- INTEL 80486DX2-66 (test date: 1995) – 0.8 um CHMOS V
  - Failure between 20-25 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/td80486.htm*
- INTEL Pentium III (test date: 2000-2) – 0.25 um
  - Failure ~500 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/G020802_P3_TID.pdf*
- AMD K7 (test date: 2002) – 0.18 um
  - Failure >100 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/G020802_P3_TID.pdf*
- ***Do we need more proof that scaling is improving digital CMOS total dose performance?***

Takeaway Thoughts

- **Digital CMOS devices**
  - **Definitely can exceed portions of the ITAR criteria tested here without any intentional radiation hardening**
- **However, multiple support/peripheral devices (i.e., surrounding the processor) failed at levels well below ITAR criteria**
  - **Likely bipolar or analog functions**
- **No *ONE* conclusion can be made whether "commercial technology is pushing the ITAR envelope inadvertently"**
  - **Depends on the technology and device, BUT the potential for some devices to "push" is there**

Summary and Acknowledgements

- We presented a representative set of total dose and dose rate data on a 32um SOI processor
  - Data shows this technology can pass certain ITAR criteria
  - Data shows that support/peripheral devices may fail certain ITAR criteria
- A new hardness assurance method was presented using commercial motherboards as "bias" and test boards – possible extension to future system on a chip (SOC) testing.
- Acknowledgements
  - NASA Electronic Parts and Packaging Program
  - NAVSEA Crane
  - Defense Threat Reduction Agency
  - National Reconnaissance Office